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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,555	04/19/2006	Hendrik Van Der Ploeg	NL03 1246 US1	3881

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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
NGUYEN, KHAI M	
ART UNIT	**PAPER NUMBER**
2819	

NOTIFICATION DATE	DELIVERY MODE
08/08/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/576,555	VAN DER PLOEG, HENDRIK	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5 and 7* is/are rejected.

7)☒ Claim(s) *3, 4, and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/19/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. An initiated copy of the information disclosure statement (IDS) submitted on 4/19/2006 is attached herewith.

Specification

3. "AD" in the title should be changed to read --analog-to-digital--. Clarification is required.

4. Continuation data should be inserted at the first paragraph of the specification.

5. The application has not been checked to the extent necessary to determine the presence of all possible typographical and grammatical errors. However, Applicant's cooperation is requested in correcting any errors of which he/she may become aware in the application.

6. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 5, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Signell et al. (US 6,028,546), hereinafter referred to as "Signell".

Regarding claim 1, Signell discloses (Figs. 1, 3-4, 7, and 9A-B) a dual (i.e., differential) residue (col. 16, lines 65-68) pipelined AD-converter for converting an analog input signal ($V_{in}^{p}(i)$ and $V_{in}^{n}(i)$) to a digital output signal (output of a comparator

53 in each stage 50), said converter comprising a cascade of dual residue converter stages (col. 14, lines 42-58), the first of said stages (50) comprising:

means (conductors/lines) to receive the analog input signal ($V_{in}^{p}(i)$ and $V_{in}^{n}(i)$);

means (comparator 53 of one stage 50 – col. 17, lines 1-5) to derive one or more digital bits (b_i) from said analog input signal; and

means (switched capacitor array of Fig. 7) to generate first and second residue signals ($V_o^{p}(i)$ and $V_o^{n}(i)$) representing the quantization error left after the AD-conversion of said first stage (col. 3, lines 56-68), each of the following stages (50) in the cascade of dual residue converter stages (50) comprising means (differential input lines of next stage 50 of the pipelined ADC) to receive the first and second residue signals ($V_o^{p}(i)$ and $V_o^{n}(i)$) generated by the previous stage in the cascade, means (comparator 53 of a next or following stage 50 of the pipelined ADC – see Fig. 4) to derive one or more further digital bits (2^{nd} MSB) from said received first and second residue signals and each of said following stages (50) except the last one (as seen in Fig. 4, the last stage 32-4 has no switched capacitor array – col. 9, lines 18-40) in the cascade comprising means (switched capacitor array of Fig. 7) to generate first and second residue signals ($V_o^{p}(i)$ and $V_o^{n}(i)$) representing the quantization error left after the AD-conversion of the stage (50), characterized in that each of the stages (50) of the dual residue pipelined AD-converter, except the last one, comprises switched capacitor means (Figs. 7, 9A, and 9B for the generation of the first and second residue signals ($V_o^{p}(i)$ and $V_o^{n}(i)$).

Regarding claim 2, Signell discloses (Figs. 1, 3-4, 7, and 9A-B) a dual (differential) residue pipelined AD-converter as claimed in claim 1 characterized in that each of said following stages (50 or 32) except the last one (Fig. 4) comprise input capacitors (capacitors C1 of Fig. 7) for receiving during a sampling phase the first and second residue signals ($V_o^p(i)$ and $V_o^n(i)$) generated by the previous stage, switching means (S1...S5 of Fig. 7) to transfer during a tracking phase (sampling phase) the charge of said input capacitors to first and second output capacitors (capacitors C2 of Fig. 7 or 9B), and means (including 51 of Fig. 7) to generate first and second residue signals ($V_o^p(i)$ and $V_o^n(i)$) from said first and second output capacitors (C2) respectively.

Regarding claim 5, Signell discloses (Figs. 1, 3-4, 7, and 9A-B) a dual residue pipelined AD-converter as claimed in claim 2 characterized in that for the generation of each residue signal an operational amplifier (51 of Fig. 7, 9A, or 9B) is provided and that each output capacitor (C2 – Fig. 9B) is connected during the tracking phase (when S2 are turned on) between an output terminal and the inverting input terminal of said operational amplifier (Fig. 9B).

Regarding claim 7, Signell discloses (Figs. 1, 3-4, 7, and 9A-B) a dual residue pipelined AD-converter as claimed in claim 1, characterized in that in that the switched capacitor means (S1...S5) are arranged to receive balanced first and second residue signals ($V_o^p(i)$ and $V_o^n(i)$) and to generate there from balanced first and second residue

signals ($V_o^p(i)$ and $V_o^n(i)$ of a following stage 50) for application to the next stage in the cascade.

Allowable Subject Matter

8. Claims 3, 4, and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the references of record neither reveal nor render obvious the recited combinations including switches that are arranged to transfer charge from the first received residue signal to the first output capacitor with a gain factor of approximately 2 and charge from both the first and second received residue signals to said second output capacitor each with a gain factor of approximately 1 in a first sub-range mode and to transfer charge from the second received residue signal to the second output capacitor with a gain factor of approximately 2 and charge from both the first and second received residue signals to the first output capacitor each with a gain factor of approximately 1 in a second sub-range mode.

Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclose (see references cited on PTO-892 Form attached herewith).

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford (Rex) Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NguyenKhai

August 1, 2007

Khai M. Nguyen
Art Unit: 2819
571-272-1809